Adaptive Matrix Multiplication for Dynamic Shapes on Ascend NPUs

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Abstract

Matrix Multiplication (MatMul) faces a "generalization crisis" driven by highly dynamic tensor shapes. This crisis is particularly acute on Ascend NPUs, where explicitly controlled architectures and strict physical constraints render existing GPU-centric optimizations ineffective. To resolve this, we propose *AdaptCore*, an adaptive framework for universally high-performance MatMul on Ascend NPUs. *AdaptCore* systematically decouples operator optimization into spatial tiling and instruction orchestration. It first maps dynamic shapes into a hardware-aware 2D tiling taxonomy to balance on-chip capacity limit and multi-core parallelism. Furthermore, it integrates a composable optimization library with a deterministic analytical performance model. By mathematically evaluating hardware state mutations, *AdaptCore* proactively selects and caches optimal implementations, enabling $O(1)$ overhead runtime dispatching. Evaluations demonstrate that *AdaptCore* delivers a remarkable 1.85× mean speedup across 80,000 input shapes, and achieves up to a 1.48× acceleration in representative end-to-end models over the highly-tuned native vendor library (ACLNN).

1 Introduction

Matrix Multiplication (MatMul) has long been the computational core of AI workloads, highly optimized for static uniform input shapes. However, as workloads become increasingly complex, MatMul operators face a severe "generalization crisis." On the one hand, input dimensions exhibit massive variance, often spanning multiple orders of magnitude (e.g., from 1 to 100,000 in recommendation scenarios [10, 16, 19]), degrading from standard square matrices to highly skewed matrices. On the other hand, emerging model architectures introduce unpredictable fluctuations to input dimensions, such as the real-time gating mechanism in Mixture-of-Experts (MoE) models [3, 7]. Consequently, traditional operators optimized for specific static shapes inevitably suffer a sharp decline in performance.

This dynamic shape crisis is particularly severe on Ascend NPUs. Unlike GPUs, which follow the SIMT paradigm and hardware-managed hierarchical memory, Ascend NPUs [4, 8] feature an explicitly managed SIMD architecture coupled with decoupled, complex memory buffers (e.g., L1 and L0 A/B/C). This requires developers to manually control instruction sequences and dependencies to ensure pipeline efficiency. Constrained by strict hardware limits and explicit control requirements, MatMul operators easily fall into a dilemma when encountering irregular dynamic shapes: either the tiles are too small, leaving compute units idle, or the tiles are too large, exceeding buffer capacity and triggering massive memory bandwidth pressure.

Unfortunately, existing operator optimizations fail to achieve both architectural awareness and runtime flexibility. High-level auto-tuning frameworks (e.g., Triton [13], cuTile [11])

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significantly lower the programming barrier but are intrinsically designed for GPUs. When ported to Ascend NPUs, they often ignore hardware characteristics, yielding sub-optimal performance and introducing search overhead. Similarly, while static template libraries (e.g., CUTLASS [12]) and specialized JIT compilers (e.g., DeepGEMM [2]) maximize hardware utilization, they either fail to handle dynamic shapes gracefully or strictly target specific hardware (e.g., Hopper).

In practice, developing such an ideal MatMul operator for dynamic shapes on Ascend NPUs is hindered by two challenges: *(i) Hardware-Constrained Tiling.* Mapping massive dynamic workloads to optimal tile sizes requires a balance between on-chip buffer capacities and multi-core parallelism. Enlarging tiles to save memory bandwidth inevitably risks buffer overflow, while shrinking them leaves compute cores starved. *(ii) Coupled Optimization Space.* Beyond tiling, fine-grained instruction optimizations (e.g., memory padding, preloading) introduce complex trade-offs. Each technique accelerates execution but also incurs inherent overheads. Without a method to quantitatively evaluate these combinatorial impacts, identifying the optimal implementation remains an open challenge.

To overcome these challenges, we propose *AdaptCore*, an adaptive framework designed for universally high-performance MatMul execution on Ascend NPUs. At its core, *AdaptCore* is driven by the insight that operator optimization can be decoupled into macro-level spatial tiling and micro-level instruction orchestration. (i) To resolve the tiling conflict between memory constraints and load balance, *AdaptCore* abandons empirical heuristics. Instead, it maps dynamic input shapes into a rigorous hardware-aware 2D taxonomy, classifying them into four base tiling templates to achieve the balance between buffer capacity and multi-core parallelism. (ii) To navigate the complex optimization space, *AdaptCore* constructs a unified analytical performance model based on Ascend's deterministic instruction pipeline. By mathematically evaluating the impact of computation, bandwidth, and pipeline optimizations, this model identifies the global optimal implementation across various tiling and optimization combinations. Finally, to seamlessly fuse these two stages for dynamic workloads, *AdaptCore* adopts a synergistic offline-online execution mechanism. In the offline phase, the analytical model proactively explores, compiles, and caches the optimal implementations into a lookup table. During online execution, *AdaptCore* achieves $O(1)$ overhead runtime dispatching through rapid shape indexing.

In summary, this paper makes the following contributions:

- We formulate MatMul tiling as a hardware-aware 2D template space defined by spatial task sufficiency and the accumulation regime, associating each shape with a template and hierarchical tiling parameters.
- We construct an analytical model and a composable optimization library to select legal optimization configurations by their data movement, resource efficiency, and pipeline schedule.
- We design an offline-selection/online-dispatch workflow that encodes each preselected implementation in a compact `TilingKey`, enabling constant-time runtime kernel lookup without online exploration.
- We evaluate *AdaptCore* on 80,000 dynamic shapes and five recommendation models. It achieves a 1.85× mean single-operator speedup over vendor library ACLNN and delivers 1.09×–1.48× end-to-end speedups.

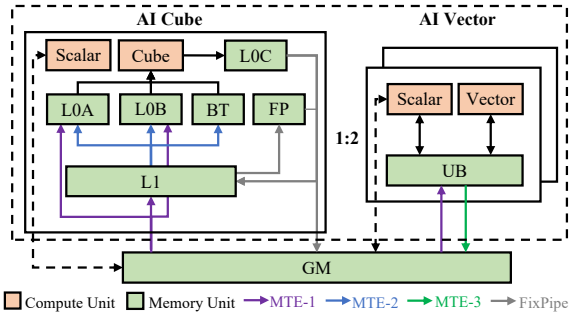


Figure 1. Architectural overview of the Ascend 910 NPU.

The rest of this paper is organized as follows. Section 2 provides the background, and Section 3 presents the system overview. Section 4 introduces the hardware-aware tiling taxonomy. Section 5 presents model-guided selection, analytical performance modeling, and the optimization library. Section 6 reports the evaluation. Section 7 discusses limitations, and Section 8 concludes.

2 Background

2.1 Ascend Architecture and Physical Constraints

To fully understand the necessity of specialized operator optimization on the Ascend architecture, we first contrast its hardware design with the dominant GPU paradigm.

GPU: Implicit Synchronization. Modern GPUs, such as NVIDIA's Blackwell architecture, employ a Single Instruction Multiple Threads (SIMT) execution model and hierarchical memory. Crucially, GPUs utilize hardware mechanisms to help developers hide memory latency and manage data flow, thereby reducing the need for explicit instruction pipeline orchestration. For example, the Tensor Memory Accelerator (TMA) autonomously fetches matrix tiles from Global Memory to Shared Memory, while hardware-level barriers (e.g., `mbarrier`) implicitly resolve dependencies.

Ascend NPU: Explicit Execution. Unlike GPUs, the Ascend NPU [8] features a deeply decoupled Single Instruction Multiple Data (SIMD) architecture. As illustrated in Figure 1,

the computational core (AICore) is composed of asynchronous units: the Cube unit (matrix multiplication), the Vector unit (element-wise), multiple Memory Transfer Engines (MTEs), and complex on-chip memory buffers, including the L1 Buffer, L0A/B/C Buffers and Unified Buffer (UB). To unlock peak performance, developers must explicitly orchestrate both the data movement across a complex on-chip memory hierarchy and the instruction synchronization.

As shown in Listing 1, the MatMul operator on Ascend consists of the following instructions: (i) The MTE2 transfers data from Global Memory (GM) to L1 Buffer. (ii) The MTE1 routes the left matrix A from L1 Buffer to L0A, and the right matrix B to L0B. (iii) The Cube unit reads operands from L0A/B to perform matrix multiplication, accumulating the results in L0C. (iv) The FixPipe (handles format conversion and post-processing) writes the results back to GM.

```
GlobalTensor<half> gm_A, gm_B; GlobalTensor<float> gm_C;
TQue<QuePosition::VECIN, 1> qL1_A, qL1_B;
TQue<QuePosition::A1, 1> qL0A;
TQue<QuePosition::B1, 1> qL0B;
TQue<QuePosition::CO1, 1> qL0C;
/* (i) GM -> L1 (MTE2) */
DataCopy(l1_A, gm_A, TSIZE); DataCopy(l1_B, gm_B, TSIZE);
qL1_A.EnQue(l1_A); qL1_B.EnQue(l1_B); // SetFlag(L1)
/* (ii) L1 -> L0A/L0B (MTE1) */
l1_A = qL1_A.DeQue<half>(); l1_B = qL1_B.DeQue<half>();
    // WaitFlag(L1)
DataCopy(l0a, l1_A, TSIZE); DataCopy(l0b, l1_B, TSIZE);
qL0A.EnQue(l0a); qL0B.EnQue(l0b); // SetFlag(L0A/B)
/* (iii) L0A, L0B -> Cube -> L0C */
l0a = qL0A.DeQue<half>(); l0b = qL0B.DeQue<half>(); //
    WaitFlag(L0A/B)
Mmad(l0c, l0a, l0b, ...);
qL0C.EnQue(l0c); // SetFlag(L0C)
/* (iv) L0C -> GM (FixPipe) */
l0c = qL0C.DeQue<float>(); // WaitFlag(L0C)
DataCopy(gm_C, l0c, TSIZE);
```

Listing 1. Abstracted Ascend C MatMul kernel

In fact, the performance of MatMul on Ascend NPUs is fundamentally impacted by two constraints: *(i) Limited Buffer Capacities.* The capacities of the dedicated on-chip buffers directly impact the efficiency of operand fetching (L0A/B) and result accumulation (L0C). In particular, if the intermediate partial sums overflow the L0C buffer, the AICore is forced to flush data back to the off-chip GM for accumulation, severely degrading the memory bandwidth. *(ii) Instruction Pipeline Efficiency.* Overall execution throughput relies heavily on how developers orchestrate instruction sequences and synchronization dependencies. For example, through fine-grained instruction optimization, we can overlap the MTE data fetching for the next block with the ongoing Cube computation to improve efficiency. Conversely, sequential execution results in poor performance.

2.2 The Dynamic Shape Crisis of MatMul

In modern AI workloads, Matrix Multiplication is no longer confined to the static, uniform input dimensions characteristic of traditional dense models. Instead, it faces two profound

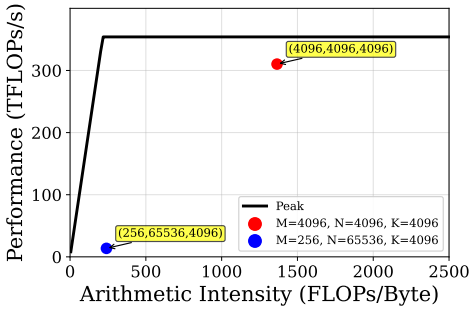


Figure 2. Roofline analysis: square vs. skewed MatMul shapes on Ascend 910.

generalization challenges: *(i) Extreme Dimensional Variance.* In industrial-scale recommendation systems, the input dimensions (M, N, K) of MatMul operators exhibit massive variance. The shape sizes can span a magnitude of over 10^5, ranging from standard square matrices to highly skewed "Tall-Skinny" or "Short-Wide" matrices. *(ii) Real-Time Dynamic Fluctuations.* Furthermore, in emerging Mixture-of-Experts (MoE) architectures, sparse activation mechanisms dynamically route tokens to a subset of experts. This real-time decision-making causes the underlying GEMM input dimensions to fluctuate unpredictably on the fly.

Consequently, operators heavily optimized for specific shapes suffer severe performance degradation when confronted with these dynamic variations. Based on the roofline analysis on Ascend NPUs in Figure 2, for a standard square matrix (e.g., $M = 4096, N = 4096, K = 4096$), a fixed tiling strategy (256×256) can perfectly balance the workload between compute units and memory units, allowing the hardware to approach its peak performance. However, when the same strategy is applied to highly irregular shapes (e.g., $M = 256, N = 64K, K = 4096$), it triggers a dual-sided hardware crisis. On the compute side, the constrained M dimension drastically reduces the computational workload per tile, leaving the Cube constantly starved for data. Concurrently, on the memory side, fetching static tiles from a large N dimension ($64K$) forces the DMA engine into inefficient strided memory accesses. This causes both compute throughput and memory bandwidth to be far below the hardware limits.

2.3 Existing Work and Limitations

To resolve the aforementioned crisis, an ideal Ascend MatMul operator must possess both deep architectural awareness and runtime flexibility. However, existing solutions fall into a Catch-22 dilemma, failing to achieve this goal.

High-Level Compilers and Auto-Tuning. OpenAI's Triton [13] and NVIDIA's cuTile [11] use auto-tuners to search for optimal block-level parallelism. While highly productive, they are intrinsically tailored to the implicit synchronization of GPUs. When ported to explicitly controlled

Ascend NPUs, they exhibit severe "architectural blindness," failing to guide an efficient instruction pipeline. Furthermore, auto-tuning may incur prohibitive search overheads when faced with the dynamic shapes in practical workloads.

Static Libraries and Specialized Compilers. Conversely, expert-level template libraries prioritize peak hardware utilization but sacrifice adaptability. For example, NVIDIA's CUTLASS [12] delivers near-handwritten performance via C++ templates, yet its rigid static configurations fail to gracefully handle extreme dynamic shapes (e.g., "Tall-Skinny" matrices). While specialized compilers like DeepSeek's DeepGEMM [2] solve this via Just-In-Time heuristics, they are locked into the specific hardware architecture (NVIDIA Hopper), offering zero portability to Ascend NPUs.

Fortunately, the native CATLASS template library [6] successfully abstracts Ascend's explicit memory routing and synchronization barriers into reusable C++ components. Rather than reinventing these intricate low-level instructions from scratch, utilizing CATLASS guarantees hardware affinity. However, it is fundamentally static. Fully unlocking its potential under dynamic irregular workloads is an challenge.

3 Overview

In this section, we first summarize core challenges in optimizing the performance of MatMul operators on Ascend NPUs, and then introduce our framework *AdaptCore*.

3.1 Core Challenges

In fact, optimizing the MatMul operator on Ascend NPUs can be distilled into solving two deeply intertwined challenges:

Challenge 1: How to select optimal tiling configurations under Ascend hardware constraints? The Ascend architecture imposes rigorous physical limitations, particularly the limited on-chip buffers (e.g., L0C) and complex coordination across multiple cores. The essence of the tiling problem lies in mapping dynamic input shapes to appropriate tile sizes. However, enlarging the tiles to save memory bandwidth inevitably breaches the on-chip memory limit, while shrinking them leads to low multi-core utilization. Given the variance in input shapes, finding the optimal tiling policy is extremely difficult.

Challenge 2: How to navigate the highly coupled, multi-dimensional optimization space? Beyond tiling, maximizing MatMul performance relies on fine-grained software optimizations, such as scalar elimination, memory padding, and preloading. These optimizations span multiple dimensions, including compute efficiency, memory bandwidth, and pipeline overlap. However, each optimization inevitably introduces inherent overheads alongside its performance gain. For example, preloading exacerbates on-chip buffer occupancy, while memory padding incurs extra format-conversion computation overhead. Composing multiple optimizations makes these performance impacts even more complex. The lack of quantitative evaluation of operator performance makes it difficult to determine an efficient operator implementation.

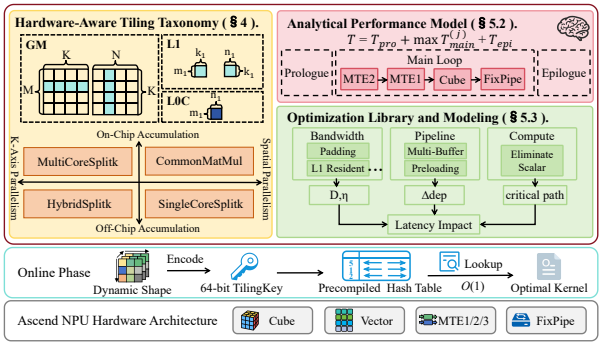


Figure 3. System overview of the proposed adaptive MatMul framework.

3.2 System Architecture

As shown in Figure 3, *AdaptCore* consists of three components that collaborate within a unified offline-online workflow.

Hardware-Aware Tiling Taxonomy (§4). *AdaptCore* systematically maps dynamic input shapes into a 2D decision space governed by Ascend hardware constraints. This taxonomy is constructed along two orthogonal dimensions: spatial parallelism (multi-core task demands) and data reuse (the L0C capacity). The two axes naturally divide the tiling space into four distinct quadrants, each representing a specific tiling template. For example, shapes with small M and N map to `MultiCoreSplitK`, splitting the K-axis to keep all AICores active. Conversely, massive read-bound shapes map to `SingleCoreSplitK`, which enlarges tiles to maximize data reuse while overflowing the L0C buffer.

Analytical Performance Model (§5.2). *AdaptCore* proposes an analytical performance model built on two abstractions of Ascend's explicit execution: (i) a three-phase decomposition of every MatMul execution into *Prologue*, *Main Loop*, and *Epilogue*; and (ii) a four-stage instruction pipeline (MTE2 → MTE1 → Cube → FixPipe) within each Main Loop iteration. Under this view, the per-iteration latency is precisely the critical-path length of this pipeline, which the model evaluates in closed form. Based on this, *AdaptCore* provides a unified analytical framework, enabling microsecond-level latency prediction without runtime profiling.

Optimization Library and Modeling (§5.3). Considering the vast optimization space, as shown in Table 2, *AdaptCore* componentizes representative optimizations into a library and categorizes them by the bottlenecks they address: (i) *Bandwidth optimizations* satisfy strict alignment constraints and manage memory hierarchies to saturate data read/write throughput. (ii) *Pipeline optimizations* manipulate the instruction streams to maximize the execution overlap between

asynchronous compute and memory units. (iii) *Compute optimizations* eliminate redundant control logic to ensure dense computing operations dominate the critical path. By feeding each module into the analytical model, *AdaptCore* quantitatively predicts its latency impact.

In practical application, *AdaptCore* comprises two distinct execution phases. During the *offline phase*, *AdaptCore* injects the composable optimization modules into specific templates, utilizes the performance model to evaluate all valid combinations, and registers the optimal kernel into a precompiled hash table named `launch_map`. During the *online phase*, *AdaptCore* encodes the incoming shape into a compact 64-bit `TilingKey`. This key serves as a direct index to perform an $O(1)$ lookup within the `launch_map`, retrieving the optimal implementation with near-zero runtime overhead.

4 Hardware-Aware Tiling Taxonomy

In this section, we first introduce the fundamental tiling principles for the MatMul operator on the Ascend NPU and systematically categorize diverse tiling scenarios into specific templates. We then present several case studies to demonstrate the superiority of tiling templates.

4.1 Rethinking Tiling on Ascend NPUs

Unlike GPUs that rely on SIMT thread schedulers to implicitly hide memory latencies, Ascend NPUs employ a decoupled SIMD design comprising independent MTE, Cube, and Vector units. Therefore, hardware synchronization, pipeline overlapping, and data transfer are not automatically managed, but explicitly governed by the tiling strategy. Here, we outline the tiling process of a MatMul operator.

As illustrated in Figure 4 and Table 1, computing an $M \times K$ by $K \times N$ matrix multiplication requires parallelizing the workload across multiple AICores, where each core handles a sub-task of size $m \times k$ and $k \times n$. Within each sub-task, the AICore processes L1 tiles of size $m_1 \times k_1$ and $k_1 \times n_1$, where $m_1 \le m$, $n_1 \le n$, and $k_1 \le k$. These tiles are further partitioned into $m_0 \times k_0$ and $k_0 \times n_0$ micro-tiles for the L0A/L0B buffers and Cube execution. The corresponding $m_1 \times n_1$ FP32 output tile is accumulated in L0C from the $m_0 \times n_0$ micro-tiles. We therefore use $m_1 n_1 \cdot 4$B, rather than the full AICore sub-task size mn, to determine whether accumulation remains on chip. If this L0C tile exceeds capacity, the AICore periodically flushes partial sums to Global Memory. Thus, m, n, k determine inter-core task partitioning, whereas m_1, n_1, k_1 determine intra-core data reuse and L0C accumulation behavior.

4.2 Design of the 2D Template Space

When mapping diverse dynamic shapes onto the Ascend NPU, a conflict emerges between inter-core load balancing and intra-core data reuse. Inter-core parallelism is determined by the AICore sub-task dimensions m, n, k, whereas

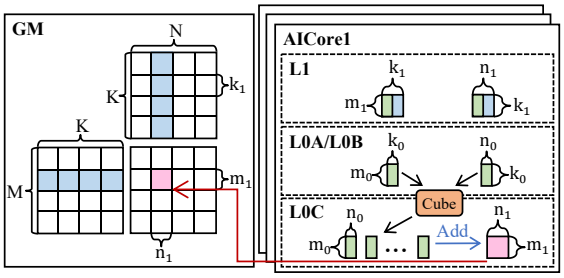


Figure 4. Multi-level tiling decomposition for MatMul on Ascend NPUs.

Table 1. Key notation.

Symbol	Description
M, N, K	Input matrix shapes.
m, n, k	AICore sub-task dimensions; they determine inter-core task partitioning. $k = K$ denotes no K-split, whereas $k < K$ denotes K-axis parallelism.
m_1, n_1, k_1	L1 tile dimensions within a sub-task. The $m_1 \times n_1$ FP32 result is L0C accumulation tile.
m_0, n_0, k_0	L0 micro-tile dimensions for L1→L0A/L0B transfers and MMAD.
$C_{L1}, C_{L0A}, C_{L0B}, C_{L0C}$	L1, L0A, L0B and L0C buffer capacities, on-chip accumulation requires $m_1 n_1 \cdot 4\text{B} \le S_{L0C}$ for FP32 results.
P_m, P_n, P_k	Task counts along M, N, K: $P_m = \lceil M/m \rceil$, $P_n = \lceil N/n \rceil$, $P_k = \lceil K/k \rceil$.

GM traffic and L0C occupancy are determined by the L1 tile dimensions m_1, n_1, k_1. Assuming FP16 inputs and no cross-tile residency, each L1 tile reads $m_1 k_1 + k_1 n_1$ elements. Summing over all tiles gives

$$D_r = 2 \cdot MNK \left(\frac{1}{m_1} + \frac{1}{n_1} \right). \tag{1}$$

Larger m_1 and n_1 improve data reuse and reduce D_r, but the resulting FP32 accumulation tile may exceed L0C capacity. Independently, larger m and n reduce the spatial task count $P_m P_n$ and may leave AICores idle. These two constraints—L0C residency and spatial parallelism—form the axes of our template space.

Because no single tiling strategy can reconcile these constraints across all shapes, *AdaptCore* organizes four template classes in the hardware-aware 2D space shown in Figure 5. The X-axis represents *Spatial Parallelism*, determined by whether the AICore task count is sufficient to saturate the cores. The Y-axis represents the *L0C Accumulation Regime*, determined by whether the FP32 L0C tile fits on chip.

Common (Spatial Parallelism, On-Chip Accumulation). This is the baseline template when spatial partitioning generates sufficient tasks to saturate all AICores ($P_m \cdot P_n \ge$

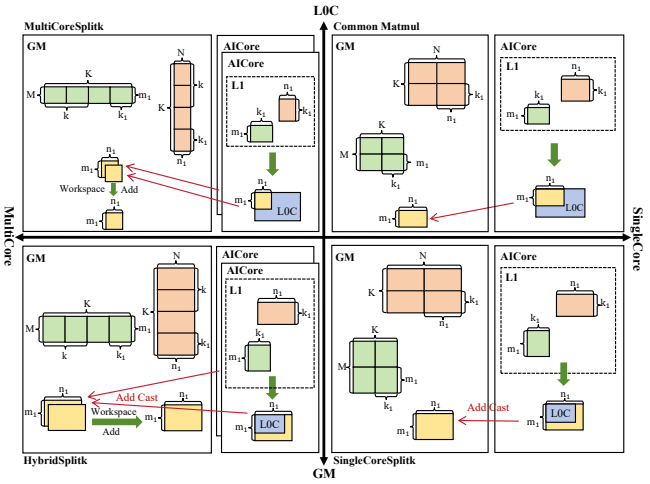


Figure 5. Hardware-aware 2D tiling template taxonomy.

N_{core}) and the L0C accumulation tile fits on chip ($m_1 n_1 \cdot 4\text{B} \leq S_{L0C}$). The entire K-dimension is processed per core ($k = K$), while each $m_1 \times n_1$ output tile is accumulated in L0C. The core performs a single FP32-to-FP16 cast and writes each final output element once to GM, yielding the minimum write volume:

$$D_w^c = 2 \cdot MN \tag{2}$$

SingleCoreSplitK (Spatial Parallelism, Off-Chip Accumulation). For read-bound matrices, *AdaptCore* enlarges m_1 and n_1 to improve L1-level data reuse, even when the resulting $m_1 \times n_1$ FP32 tile exceeds L0C capacity. The entire K-dimension remains assigned to one core ($k = K$), but the core flushes intermediate partial sums after each k_1 slice. This template trades increased write volume for reduced GM read volume:

$$D_w^s = 4 \cdot MN \left\lceil \frac{K}{k_1} \right\rceil + 2 \cdot MN \tag{3}$$

MultiCoreSplitK (K-Axis Parallelism, On-Chip Accumulation). For compute-underutilized shapes (e.g., tall-skinny matrices), $P_m P_n < N_{core}$ leaves AICores idle. This template partitions the K-dimension across multiple cores ($k < K$), while each local $m_1 \times n_1$ FP32 tile still fits in L0C. Every K-partition exports one partial result to GM for cross-core reduction, so the write volume depends on the partition count P_k:

$$D_w^m = 4 \cdot MN \left\lceil \frac{K}{k} \right\rceil + 2 \cdot MN \tag{4}$$

HybridSplitK (K-Axis Parallelism, Off-Chip Accumulation). This template combines `SingleCoreSplitK` and `MultiCoreSplitK` when spatial tasks cannot saturate all AICores ($P_m P_n < N_{core}$) and the enlarged L0C tile exceeds capacity ($m_1 n_1 \cdot 4\text{B} > S_{L0C}$). It partitions the K-axis across $P_k > 1$ cores while using large m_1, n_1 tiles for data reuse. Each AICore consequently flushes local partial sums after every k_1 slice, giving:

$$D_w^h = P_k \times \left(4 \cdot MN \cdot \left\lceil \frac{k}{k_1} \right\rceil\right) + 2 \cdot MN = 4 \cdot MN \cdot \left\lceil \frac{K}{k_1} \right\rceil + 2 \cdot MN \tag{5}$$

While its mathematical write volume is identical to Equation 3, this massive memory penalty is distributed concurrently across P_k AICores.

In summary, these four templates establish a complete design space to balance data transfer volumes and multi-core utilization. Furthermore, these templates can be combined with other tiling strategies to handle extreme cases. For example, the StreamK strategy can be applied to existing templates to address the tail-iteration load imbalance problem.

4.3 Mapping Shapes to Templates

In practice, standard shapes often fall into the `Common` quadrant. If the enlarged tiles overflow the L0C buffer, execution shifts to `SingleCoreSplitK`. Conversely, if the shape lacks spatial parallelism, the system triggers `MultiCoreSplitK` to partition the K-axis. Finally, shapes suffering from both core starvation and L0C overflow land in the `HybridSplitK`. Here, we provide four representative tiling cases on an Ascend NPU equipped with 16 AICores and a 128 KB L0C. Note that the accumulation on L0C uses the Float32 data type.

Case 1: Well-Balanced Workload. For $M = N = K = 1024$, let each AICore task contain one L1 output tile with $m = m_1 = 128$ and $n = n_1 = 256$. The FP32 L0C tile occupies exactly 128 KB, while the spatial partitioning generates $(1024/128) \times (1024/256) = 32$ tasks for 16 AICores. The `Common` template therefore provides both on-chip accumulation and sufficient parallelism.

Case 2: Read-Bound Large Matrices. For $M = N = 4096$ and $K = 1024$, increasing the L1 tile from $m_1 \times n_1 = 128 \times 256$ to 256×256 reduces D_r but enlarges the FP32 L0C tile from 128 KB to 256 KB. With $k = K$ and sufficient spatial tasks, this selects `SingleCoreSplitK`: the larger L1 tile improves reuse, while partial sums are accumulated off chip.

Case 3: Compute Underutilization for Skewed Shapes. For $M = N = 128$ and $K = 4096$, let $m = m_1 = n = n_1 = 64$. The 16 KB FP32 L0C tile fits on chip, but the spatial partitioning yields only $(128/64)^2 = 4$ tasks, leaving 12 of 16 AICores idle. Splitting K across the idle cores selects `MultiCoreSplitK` and improves parallelism at the cost of cross-core reduction.

Case 4: Skewed-Massive Shapes. For $M = N = 256$ and $K = 8192$, let $m = m_1 = n = n_1 = 256$. The configuration produces only one spatial task and a 256 KB FP32 L0C tile. It therefore violates both conditions, selecting `HybridSplitK` to combine K-axis parallelism with off-chip accumulation.

5 Optimization Space Exploration

Although base tiling templates bring substantial performance improvements, achieving peak performance still relies on

complex instruction-level optimizations. In this section, we detail how *AdaptCore* decouples these optimizations into pluggable components applied to the templates. We also introduce a lightweight cost model to evaluate the benefits of applying the optimizations, guiding developers to choose the optimal operator implementation.

5.1 Model-Guided Candidate Selection

Given an input shape $s = (M, N, K)$, the 2D taxonomy in Section 4.2 deterministically produces a base implementation $b(s) = (q(s), \boldsymbol{\theta}(s))$, where $q(s)$ is one of the four templates and $\boldsymbol{\theta}(s) = \{m, n, k, m_1, n_1, k_1, m_0, n_0, k_0\}$ contains its associated tiling parameters. Based on this, *AdaptCore* explores a set $\mathcal{S}(b(s))$ of compatible optimization configurations. Each configuration $\mathbf{x}$ specifies both the enabled optimizations and their internal choices, such as the padding format and preloading depth. *AdaptCore* rejects configurations that violate instruction requirements or any capacity limit in the explicitly managed memory hierarchy. Let $\mathbf{M}(b, \mathbf{x}, s)$ denote the resulting footprint across the L1 and L0A/B/C buffers, and let $\mathbf{C}_{limit}$ denote their hardware capacities. *AdaptCore* selects the configuration with the minimum latency predicted by its analytical model $\widehat{T}$:

$$\mathbf{x}^*(s) = \underset{\mathbf{x}\in\mathcal{S}(b(s))}{\arg\min}\ \widehat{T}(b(s), \mathbf{x}, s) \quad \text{s.t.} \quad \mathbf{M}(b(s), \mathbf{x}, s) \preceq \mathbf{C}_{limit}. \tag{6}$$

The exploration is performed offline for the target shape set. The selected optimization configuration, together with its predetermined template and tiling parameters, is encoded into a compact `TilingKey` and cached with the generated kernel. At runtime, *AdaptCore* only maps the incoming shape to its key and retrieves the corresponding kernel.

5.2 Analytical Performance Modeling

Given the base implementation $b(s)$ and an optimization configuration $\mathbf{x}$, *AdaptCore* predicts latency by decomposing execution into a Prologue, a parallel Main Loop, and an Epilogue:

$$\widehat{T}(b, \mathbf{x}, s) = T_{pro} + \max_{j\in\mathcal{P}} T^{(j)}_{main} + T_{epi}, \tag{7}$$

where $\mathcal{P}$ is the set of participating AICores. The maximum captures the fact that kernel completion is determined by the slowest core.

Resource Cost. For a transfer stage r, its latency on a tile v is modeled as

$$t_{r,v} = n_{r,v}\lambda_r + \frac{D_{r,v}}{BW_r\eta_{r,v}}, \tag{8}$$

where $n_{r,v}$ and $D_{r,v}$ are its instruction count and transferred bytes, BW_r is the peak bandwidth, and λ_r and $\eta_{r,v}$ denote the per-instruction overhead and the shape- and alignment-dependent hardware efficiency, respectively. We obtain λ_r and $\eta_{r,v}$ through empirical offline latency profiling. Cube latency is similarly computed as $t_{cube,v} = N_{mmad,v}\lambda_{mmad}$, where $N_{mmad,v}$ is derived from the L0 tiling parameters. Equation 8 evaluates an optimization by propagating its effects on data volume, instruction count, and hardware efficiency.

Prologue. The Prologue contains optional preprocessing before the kernel main loop. For example, Padding reads an input through MTE2, reformats it on the Vector unit, and writes the transformed data through MTE3. We compute T_{pro} by summing these dependent stages using Equation 8; $T_{pro} = 0$ when no preprocessing is required.

Main Loop. Let $\mathcal{V}_j$ be the set of L1-level tile instances assigned to core j. Each tile v produces an output region of at most $m_1 \times n_1$ and processes its local K range in $L_v = \lceil k_v/k_1 \rceil$ slices. A slice follows the deterministic MTE2–MTE1–Cube pipeline, with FixPipe additionally appearing as a recurring stage when partial sums must be spilled from L0C.

For a given template and optimization configuration, the steady-state initiation interval is

$$II_v(b, \mathbf{x}) = \max_{r\in\mathcal{R}_b} t_{r,v} + \Delta_{dep,v}(b, \mathbf{x}), \tag{9}$$

where $\mathcal{R}_b$ is the set of recurring hardware stages and $\Delta_{dep,v}$ is the exposed latency caused by data dependencies, synchronization, and buffer reuse hazards. Multi-buffering and preloading reduce $\Delta_{dep,v}$ by enabling overlap across adjacent slices, but are enabled only when the capacity constraint in Equation 6 remains satisfied.

Accounting for pipeline fill, steady-state execution, and drain, the main-loop latency is

$$T^{(j)}_{main} = \sum_{v\in\mathcal{V}_j} \left[T_{fill,v} + (L_v - 1)II_v + T_{drain,v}\right]. \tag{10}$$

For `Common` and `MultiCoreSplitK`, accumulation remains on chip, so FixPipe is excluded from II_v and its final write is included in $T_{drain,v}$. For `SingleCoreSplitK` and `HybridSplitK`, L0C overflow causes periodic partial-sum spills, making FixPipe a recurring stage in $\mathcal{R}_b$. Boundary tiles and the last K slice are evaluated using their actual dimensions.

Epilogue. The Epilogue contains only post-processing required by the selected template and modules:

$$T_{epi} = T_{local\_reduce} + T_{cross\_reduce} + T_{format}. \tag{11}$$

`SingleCoreSplitK` requires local reduction of off-chip partial sums, `MultiCoreSplitK` requires cross-core reduction, and `HybridSplitK` requires both; the corresponding terms are zero for `Common`. Format conversion are included only when activated. Each term is evaluated from its data movement and Vector instruction costs using Equation 8.

5.3 Optimization Library and Modeling

AdaptCore componentizes common techniques from expert-tuned kernels into the optimization library summarized in Table 2. The modules target three bottleneck dimensions.

Bandwidth modules change transferred bytes D or bandwidth efficiency η; *pipeline* modules reduce the exposed dependency latency Δ_{dep}; and *compute* modules remove inefficient compute instructions from the critical path. Our analytical model can evaluate their benefits and penalties, both individually and in combination.

Pipeline Optimization Modeling. We use double buffering and preloading to illustrate how the model evaluates pipeline optimizations. As shown in Figure 6, these optimizations preserve the transferred bytes and MMAD count, but change the instruction dependencies and buffer footprint. For an L1 tile v, let $t_{M,v} = t_{mte2,v}$ denote the MTE2 time of one K-slice and let $t_{P,v} = \max(t_{mte1,v}, t_{cube,v})$ denote the overlapped L0/Cube pipeline time. The tile contains L_v slices.

Baseline. As shown in Figure 6a, the same buffer cannot be refilled until its MTE1/Cube consumers finish. MTE2 and the L0/Cube pipeline are serialized across slices, giving

$$T_v^{base} = L_v(t_{M,v} + t_{P,v}) + T_{drain,v}. \quad (12)$$

Double Buffering. Figure 6b alternates two buffer stages in a ping-pong manner. While MTE1/Cube consumes one stage, MTE2 fills the other. After the initial fill, consecutive slices are issued every $\max(t_{M,v}, t_{P,v})$ cycles:

$$T_v^{db} = t_{M,v} + (L_v - 1)\max(t_{M,v}, t_{P,v}) + t_{P,v} + T_{drain,v}. \quad (13)$$

Thus, the initiation interval in Equation 9 becomes $II_v^{base} = t_{M,v} + t_{P,v}$ for the baseline and $II_v^{db} = \max(t_{M,v}, t_{P,v})$ for double buffering.

Preloading. Double buffering still pays an MTE2 fill at the beginning of every L1 tile. Figure 6c advances the first MTE2 transfer of tile $v+1$ into the L0/Cube pipeline of tile v. For Q_j regular tiles assigned to core j, each containing L slices with stage times t_M and t_P, the continuous pipeline is modeled as

$$T_{main,reg}^{(j),pre} = t_M + (Q_j L - 1)\max(t_M, t_P) + t_P + Q_j T_{drain}. \quad (14)$$

In contrast, double buffering executes the same tiles in $Q_j[t_M + (L-1)\max(t_M, t_P) + t_P + T_{drain}]$.

The model substitutes Equations 12–14 into the latency model and selects the fastest legal schedule. Double buffering or preloading is rejected if it violate hardware limits. The remaining optimizations in Table 2 are evaluated analogously by updating their affected model variables.

6 Evaluation

In this section, we evaluate the performance of the MatMul operators generated by *AdaptCore* against baselines on Ascend. We also conduct comprehensive scalability and ablation studies to demonstrate *AdaptCore*'s effectiveness.

6.1 Experimental Setup

Hardware. The evaluation of our MatMul templates was conducted on Linux servers equipped with Huawei Ascend 910B NPUs. Each NPU card accommodates 24 AICores, delivering a theoretical peak FP16 compute throughput of 376 TFLOPS and an off-chip Global Memory (GM) to L1 Cache bandwidth of approximately 1.6 TB/s.

Software. The detailed software environment included CANN 9.0.T500, Python 3.13.11, CMake 3.31.10, Clang 15.0.5, and GCC 10.3.1. We utilized the `msprof` profiling tool included in the CANN package to collect hardware metrics and execution traces during operator runtime.

Baselines. We compared *AdaptCore*'s MatMul operator implementations with those provided by the Ascend vendor library (ACLNN [5]) and the basic CATLASS templates [6]. Given high auto-tuning overhead and the lack of awareness regarding the Ascend memory architecture, the latency of Triton-Ascend [14] operators is currently far higher than that of the aforementioned options. Therefore, it is not being considered. By comparing the practical execution times of these implementations, we demonstrate the generalization capability and effectiveness of *AdaptCore*.

Workloads. To comprehensively assess the effectiveness, we evaluated the single-operator latency and end-to-end latency of real-world recommendation scenarios, which are heavily affected by dynamic input shapes. For single-operator latency, we construct a large-scale dataset of roughly 80,000 diverse and dynamic MatMul input shapes derived from real-world industrial input ranges and distributions. For end-to-end performance, we benchmark inference workloads from representative recommendation models, including MMOE [17], DLRM [10], DCN V2 [15], ESMM [9], and RankMixer [20].

6.2 Single-Operator Latency

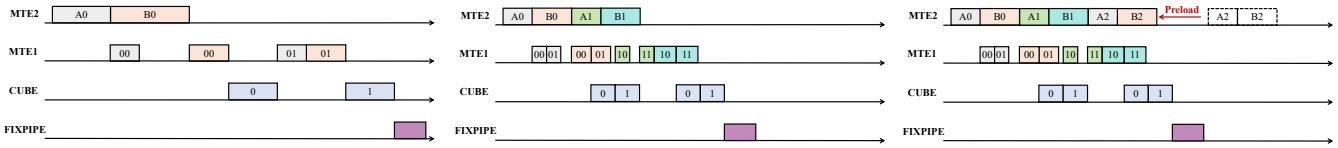
Figure 7 visualizes the distribution of approximately 80,000 input shapes in the 3D (M, N, K) space with their assigned tiling templates. The dataset spans regular to extreme shapes, fully capturing the variance of dynamic workloads. Through its hardware-aware taxonomy, *AdaptCore* maps these shapes to distinct templates, revealing clear shape characteristics. For example, shapes with a large K dimension favor the `MultiCoreSplitK` template to maximize multi-core parallelism, while shapes with larger M and N dimensions tend to use `SingleCoreSplitK` to optimize memory bandwidth. Finally, due to its strict triggering conditions, the `HybridSplitK` template is rarely activated, appearing only 591 times.

We compare the operator execution latency of three implementations: the ACLNN library, basic CATLASS template library, and *AdaptCore*. Unlike the hand-tuned ACLNN implementation, basic CatLASS exposes explicit tiling primitives but requires the user to manually select the template and schedule the pipeline.

Figure 8 quantifies the hardware utilization of different operator implementations for these dynamic shapes. The Roofline-style plot summarizes the performance distribution of four GEMM implementations. The median performance

Table 2. Composable optimization modules and their effects.

Dimension	Optimization	Benefit	Cost or constraint
Bandwidth	Padding	Improves MTE2 efficiency through 512B-align.	Adds padded traffic and format conversion.
	L1 Resident	Reduces GM-to-L1 traffic by reusing the operand.	Increases the L1 footprint.
	ShuffleK	Improves effective GM bandwidth by staggering inter-core accesses.	May increase TLB pressure; benefit is shape-dependent.
	Small-M Copy	Reduces conversion and MTE instruction overhead for narrow matrices.	Adds specialized scalar control and applicability constraints.
Pipeline	Multi-Buffer	Reduces Δ_{dep} by alternating independent buffers.	Multiplies the corresponding L1/L0 footprint.
	Preloading	Reduces Δ_{dep} and repeated fill cost by advancing the next transfer.	Requires additional L1 stages.
Compute	Eliminate Scalar	Reduces control instructions on the critical path.	Specializes the kernel and increases code variants.



(a) Baseline. **(b)** Double-Buffer. **(c)** Preloading.

Figure 6. Comparison of three pipeline schedules and their effects on buffer-reuse hazards.

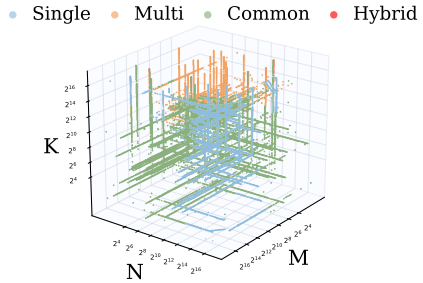


Figure 7. Statistical distribution of input shapes.

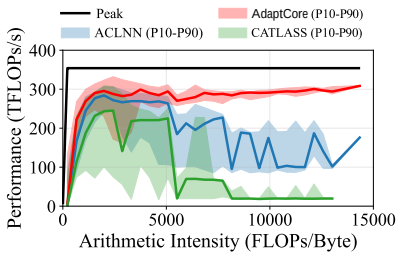


Figure 8. Roofline model of different Matmul.

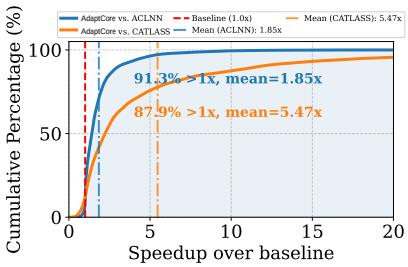


Figure 9. CDF of speedup.

(solid lines) and P10–P90 interval (shaded areas) are computed via arithmetic intensity binning, enabling a robust comparison of both peak throughput and performance variability. Relying on static tiling rules, the baseline ACLNN operator severely underutilizes both compute and memory bandwidth when encountering irregular shapes (blue), achieving an average throughput of only 71.50 TFLOPs/s. In contrast, *AdaptCore* significantly boosts both arithmetic and memory bandwidth utilization (red), driving the average throughput up to 90.96 TFLOPs/s. Meanwhile, the basic CATLASS matmul (green) achieves an average throughput of 55.81 TFLOPs/s on dynamic shapes, Both the baselines fall considerably behind *AdaptCore*.

The CDF of latency-speedup in Figure 9 also confirms the trend: *AdaptCore* achieves a mean speedup of 1.85× over ACLNN, and 5.47× over basic CATLASS The largest gains occur on highly skewed shapes, for which generic template and pipeline choices leave substantial hardware resources underutilized.

6.3 Ablation Study

To evaluate the performance gains from *AdaptCore*'s tiling templates and composable optimizations, we conduct an ablation study on a representative regular shape ($M = 12288$, $N = 688$, $K = 16991$). As illustrated in Figure 10, using the native ACLNN implementation (3246.0 μs) as the baseline, we incrementally activate optimizations. First, applying the

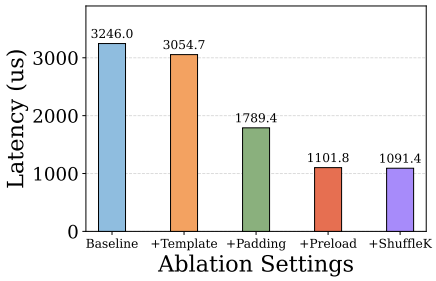


Figure 10. Ablation analysis on a representative skewed shape.

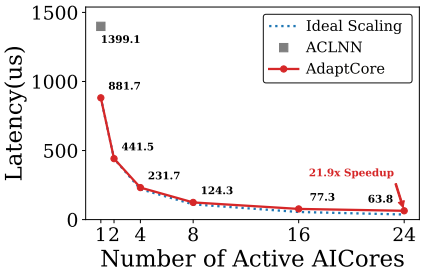


Figure 11. Multi-core scalability analysis.

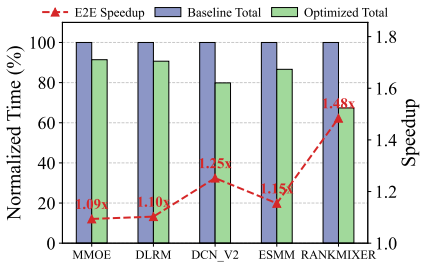


Figure 12. Latency reduction of end-to-end latency.

Common Template slightly reduces latency to 3054.7 μs by automatically deriving optimal tiling parameters for this uniform shape. Next, integrating *Memory Padding* drastically cuts the latency to 1789.4 μs. This optimization uses the Vector unit to pre-transform the right matrix into the NZ format and aligns the stride to 512B, strictly matching the L1 buffer layout. This eliminates the massive bandwidth degradation caused by unaligned memory accesses and ND-to-NZ format conversions. Building on this, we enable *Preloading* ($p = 1$) to perfectly overlap Cube computation with GM to L1 data fetches. This pipelining effectively hides the memory latency, further dropping the execution time to 1101.8 μs. Finally, we apply *ShuffleK*, which temporally staggers the data access sequence to prevent concurrent read conflicts across multiple AICores. However, since the read bandwidth is already near-optimal due to previous steps, the latency yields a marginal reduction to 1091.4 μs. Overall, these results strongly validate the effectiveness of *AdaptCore*'s tiling templates and composable optimizations.

6.4 Scalability Analysis

To evaluate *AdaptCore*'s impact on multi-core parallelism efficiency, we conduct a comprehensive scalability study. We select a highly skewed shape with a large K dimension ($M = 3, N = 256, K = 87087$) and scale the number of available AICores on the Ascend NPU from 1 to 24 to monitor latency variations. As illustrated in Figure 11, the native ACLNN implementation suffers from a severe scalability bottleneck. Constrained by static tiling rules, the total number of parallel tasks in ACLNN is strictly limited by the minuscule M and N dimensions. Consequently, it activates only a single core (yielding a latency of 1399.1 μs) and leaves the remaining 23 AI Cores completely idle, failing to extract any scaling benefits. In contrast, *AdaptCore* leverages its hardware-aware taxonomy to dispatch the `MultiCoreSplitK` template. By partitioning the massive K axis and coordinating inter-core reductions, *AdaptCore* achieves exceptional load balancing and sustained latency reductions. Its execution time scales near-ideally, plunging from 881.7 μs on a single core down to 63.8 μs on 24 cores. At full 24-core utilization, *AdaptCore* delivers a massive 21.9× speedup over the native baseline.

6.5 End-to-End Latency

To evaluate the end-to-end benefits of *AdaptCore* in real-world scenarios, we benchmark the inference latency across representative recommendation models (e.g., MMoE, DLRM, DCN V2, ESMM, and RankMixer). By seamlessly replacing the native General Matrix Multiply (GEMM) operators (including standard MatMul, AddMM, GroupMM, and BatchMM) with *AdaptCore* 's implementation, we observe substantial speedups in end-to-end time. As illustrated in Figure 12, we present the normalized execution time breakdown and the corresponding speedups. In the ACLNN implementation of different models, GEMM operators are the primary bottleneck. Following our optimization, the latency of these GEMM operators is drastically compressed while the non-GEMM operators remain constant. Eliminating the GEMM bottleneck yields the 1.09×-1.48× speedups of end-to-end latency.

6.6 Performance Model

We first evaluate the prediction accuracy of the analytical model. Because the model is designed to rank candidate configurations rather than predict cycle-accurate absolute latency, moderate point-wise error is expected. On the 80,000-shape benchmark, we exhaustively measure all valid template–optimization configurations and treat the fastest as the oracle. *AdaptCore* selects the exact oracle configuration for 63.86% of the shapes. Importantly, the selected kernels still outperform ACLNN on 91.3% of the shapes, confirming that the model-guided ranking is effective in practice.

We then measure the deployment cost of the cost model. The model is invoked only at template selection time, before operator kernel generation. Its main overhead comes from evaluating the performance formulas for each candidate strategy and checking capacity constraints. The average modeling time per shape is on the order of 10 milliseconds. Since this process can be performed offline, its cost remains acceptable even for a dataset of 80,000 shapes. This confirms

that *AdaptCore*'s analytical model is practical for deployment.

7 Limitations and Future Work

We list the current limitations of *AdaptCore* and outline several directions for future exploration.

Architectural Generality. While the methodology of *AdaptCore* (hardware-aware tiling taxonomy and optimization modeling) is theoretically generalizable, its specific templates and empirical estimates heavily rely on Ascend hardware. Porting *AdaptCore* to other Domain-Specific Architectures (DSAs) with different memory hierarchies would require redefining the taxonomy and analytical performance models.

Operator Scope and Workload Shifts. Currently, *AdaptCore* focuses on matrix multiplication operators (e.g., MatMul, GroupMM, BatchMM). As AI workloads evolve towards ultra-low precision (FP8/INT4), highly unstructured sparsity, or complex operator fusion, execution bottlenecks may shift. Moving forward, we plan to extend our methodology to a broader spectrum of complex operators (e.g., FlashAttention, Convolution) by formalizing their hardware constraints.

Agent-Driven Operator Generation. Recent research has explored the use of LLM agent workflows (e.g., CUDA Agent [1], TensorCoder [18]) for auto kernel generation. However, due to a lack of hardware knowledge of Ascend NPUs and reliable training data, these models perform poorly on Ascend. In the future, we aim to integrate our architectural insights into an Ascend operator agent to assist efficient bottleneck localization, bug elimination, and performance tuning.

8 Conclusion

In this paper, we propose *AdaptCore* to resolve the severe dynamic shape crisis on explicitly decoupled Ascend NPUs. By introducing a hardware-aware 2D tiling taxonomy, an analytical performance model and a composable optimization library, *AdaptCore* mathematically navigates strict physical constraints to achieve $O(1)$ optimal runtime dispatching. Comprehensive evaluations across 80,000 industrial shapes and representative end-to-end models demonstrate that *AdaptCore* delivers a remarkable 1.85× mean speedup over native vendor libraries. Ultimately, *AdaptCore* successfully bridges deep architectural awareness with runtime flexibility, establishing a new paradigm for universally high-performance AI execution on explicitly controlled hardware.

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